REMARKS/ARGUMENTS

The drawings were objected to.

The drawings have been amended to overcome the objections. The specification has been amended to describe the changes made to the drawings. No new matter has been added to the specification. The added features were described in the specification as filed.

Claims 9-11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Tran; claims 5-7 and 13-15 stand rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Han.

Claim 9 comprises the limitation of a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor. In forming the rejection for claim 9 the examiner has cited the Tran patent. In Figure 3 the Tran patent shows a pull up transistor 72, a pull down transistor 74, and pass transistors 76 connected between the common nodes A and B. In forming the rejection the examiner has incorrectly included the pass transistors 76 in the pull down network. In describing transistors 76, the Tran patent in col. 4, lines 55-58 describes 76 in Figure 3 as a passing gate. The examiner should be aware that in the circuit arts the terms pull up transistor 72, pull down transistor 74, and passing gates 76 are terms of art that have clearly defined meanings. In describing the circuit in Figure 3, the Tran patent has used the terms according to their well understood and established meanings. It is therefore quite clear that the feature 76 is a pass gate and is not a part of the pull down network which in the case of the circuit shown in Figure 3 consists of transistor 74. Claim 9 is therefore allowable over the Tran patent. Claims 10 and 11 depend on claim 9 can contain all the limitations of claim 9. Claims 10 and 11 are therefore also allowable over the cited art.

Claim 5 comprises the limitation of a pull-down network comprising a plurality of series connected PMOS transistors. The Han et al. reference shows a CMOS domino logic circuit and not a dynamic logic circuit as incorrectly stated by the examiner. The domino logic circuit uses clock signals to switch the pull up transistors (PMOS devices for charging 411-1, 411-2) and pull down transistors (NMOS devices for discharging 423-1, 423-2). The reference describes the blocks 412-1, 412-2, 422-1, and 422-2 as NMOS and PMOS logic blocks respectively. It is not inherent in a "logic block" just what the internal connections of the transistors are since the "logic block" encompasses all possibilities. Claim 5 is allowable over the cited art. Claims 6 and 7 depend on claim 5 and contain all the limitations of claim 5. Claims 6 and 7 are therefore also allowable over the cited art.

Claim 13 comprises the limitation of a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node. The Han et al. reference shows a CMOS domino logic circuit and not a dynamic logic circuit as incorrectly stated by the examiner. The domino logic circuit uses clock signals to switch the pull up transistors (PMOS devices for charging 411-1, 411-2) and pull down transistors (NMOS devices for discharging 423-1, 423-2). The reference describes the blocks 412-1, 412-2, 422-1, and 422-2 as NMOS and PMOS logic blocks respectively. It is not inherent in a "logic block" just what the internal connections of the transistors are since the "logic block" encompasses all possibilities. Claim 13 is allowable over the cited art. Claims 14 and 15 depend on claim 13 and contain all the limitations of claim 13. Claims 14 and 15 are therefore also allowable over the cited art.

Applicant appreciates the indication that claims 1-4 are allowed.

Applicant further appreciates the indication that claims 8, 12 and 16 would be allowable if rewritten in independent form including all of the limitations of the base

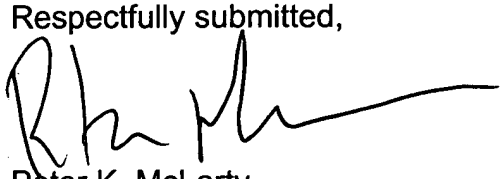
claim and any intervening claims. Claims 8, 12, and 16 were amended to include the limitations of the base claims.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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